IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First Named Inventor :	Errol C. Heiman et al.	Appeal No. ---
Appln. No. :	09/823,079	Confirmation No. 6981
Filed :	March 30, 2001	Group Art Unit: 2161
For :	COMPREHENSIVE APPLICATION POWER TESTER	Examiner: Etienne Pierre Leroux
Docket No.:	S01.12-1022	

REPLY BRIEF

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Sir:

This is in response to the Examiner's Answer dated March 17, 2009.

In section 10 (Response to Argument section) of the Answer, the Examiner, in general, treats structural claim elements, such as the additional power source, as functional. Based on this incorrect characterization of the claim elements, the Examiner proceeds to argue that a single power source that is capable of providing multiple voltage levels, taught by Hallberg, is equivalent to the multi-voltage power source and the additional power source of the claimed invention.

In an attempt to demonstrate that Hallberg shows both a "multi-voltage power source" and an "additional power source" as featured by claim 18, the Office Action combines a multi-voltage power source from one embodiment (described in column 2, lines 55-63, cited in the Office Action) with a multi-voltage power source of a different embodiment (described in column 10, line 66 through column 11, line 12, cited in the Office Action). All embodiments of Hallberg include only one power source that is capable of providing multiple voltage levels. No embodiments describe both a "multi-voltage power source" and an "additional power source" as featured by claim 18. None of Hallberg's embodiments even remotely suggest using multiple power sources. Thus, an attempt to combine different examples of a single power source in Hallberg to reject an invention with multiple power sources is improper.

The Examiner responded to this argument in the Reply Brief by stating the following:

> Examiner maintains the preferred method and the alternate embodiment disclosed by Hallberg may be combined because the alternate embodiment supplements the preferred method while no conflict is produced. The preferred method includes "at least two different voltages" and therefore, a third voltage, i.e., of the alternate embodiment, may be included because the preferred method is **not** (emphasis added) restricted to two and only two voltages. Furthermore, the alternate embodiment includes a first voltage, a second voltage and a third voltage. Clearly, the at least two different voltages of the preferred method can be substituted for the first voltage and the second voltage of the alternate embodiment.

Appellant respectfully points out that since Hallberg's single power source in the alternate embodiment is already capable of providing three voltage levels, there would be no reason to replace that single power source in Hallberg with one power source that supplies two voltage levels and a second power source that supplies one voltage level. The reasoning provided in the above argument from the Examiner's Answer is thus contrary to the teachings of Hallberg.

Also, as indicated above, any suggestion that the claimed additional power source is merely functional is incorrect. As noted in the Statement in the Response to Notice of Non-Compliant Appeal Brief, FIG. 1 of the Appellant's specification explicitly shows two separate power sources 107 and 108, and paragraph 19 of the specification explicitly describes these two separate power sources. Thus, the claimed additional power source is a structural element.

In summary, the entire Hallberg reference includes nothing about two different power sources, such as the "multi-voltage power source" and the "additional power source," which are included in claim 18.

As noted in the Appeal Brief, the Office Action correctly points out that Hallberg does not disclose circuitry configured to introduce controllable disturbances into a constant power supply voltage. In fact, Hallberg makes no suggestion of that feature. As a result, the Office Action relies on Ehiro (citing FIGS. 1, 4 and 5, column 7, lines 10-50, column 2, lines 15-20).

On page 13 of the Answer, the Examiner states that "the claim 18 limitation 'constant power supply voltage' is anticipated by VDD = 5.00 V as disclosed by Ehiro." The Examiner then suggests that the claimed "controllable disturbances in the constant power supply voltage"

are shown in FIG. 5 of Ehiro "because the disturbances cause the nominal 5.00 Volt power supply to become 4.99V, 4.98V, 4.97V." This statement is incorrect because the 5.00-Volt level shown in FIG. 5 of Ehiro is unrelated to the power supply voltage VDD in Ehiro.

In formulating the portion of the rejection based on Ehiro, in general, the Examiner treats claim elements and portions of claim elements in isolation, without taking into consideration where the constant power supply voltage is supplied from. Claim 18 features "a multi-voltage power source . . . supplying . . . a constant power supply voltage at a nominal power supply voltage of an electronic device," and "circuitry configured to introduce controllable disturbances into the constant power supply voltage." Column 7, lines 30-50, of Ehiro, are as follows:

> "FIG. 5 shows a signal waveform in the function test 2 at step a20 in FIG. 3. The clock signal fed as an input signal to the DUT 2 is a repeating signal decreasing in peak voltage to 0.00 V side at every step by 0.01 V, with a reference voltage of 5.00 V. In the range where the peak voltage exceeds the threshold VTH2, state transition of the Schmitt circuit 21 does not take place, and the current flowing in the DUT 2 hardly changes, and the input signal detected by the resistance 41 and fed to the set input terminal S of the latch circuit 46 is hardly changed. At test step M+1 where the peak voltage of the clock signal is smaller than the threshold VTH2, a large power source current flows due to state transition of the Schmitt circuit 21, and the input signal detected by the resistance 41 and fed to the set input terminal S of the latch circuit 46 comes to exceed the input inversion level of the latch circuit 46. As a result, after test step M+1, the output of the latch circuit 46 is changed from the state of low level reset in the initial setting to the state of high level. The output level of the latch circuit 46 is detected by the control circuit 16 in the comparator 15 at the test timing shown in FIG. 5." (Emphasis Added.)

The immediately preceding section (Column 7, lines 11-29) of Ehiro is as follows:

> "FIG. 4 shows the operation timing of the function test 1 at step a10 in FIG. 3. The input signal of the DUT 2 becomes a pulse signal increasing in peak voltage by 0.01 V at every test step, with a reference voltage of 0.00 V. Until test step N, the peak voltage does not reach the first threshold VTH1, and the Schmitt circuit 21 does not cause state transition. Accordingly a signal to be entered in the set input terminal of the latch circuit 46 is hardly generated.

> At test step N+1, since the peak voltage of the clock signal exceeds the threshold VTH1, a large power source current on the basis of the state transition of the Schmitt circuit 21 flows, which is detected as a voltage drop of the resistance 41, and an input signal exceeding its input inversion level is fed also to the set input terminal S of the latch circuit 46, and the output level of the latch circuit 46 reset in the initial setting is changed to high level. The output level of the latch circuit 46 is judged at the strobe point of test timing given to the comparator circuit 15, and at test step N+1 the output level is ascertained to exceed the threshold VTH1." (Emphasis Added.)

From the above sections of Ehiro, it is clear that the reference voltage for the clock input can have different values (such as 0 Volts and 5 Volts) and has nothing to do with the power supply voltage VDD, in Ehiro, applied to the device under test (DUT) 21. As noted in the Appeal Brief, in Ehiro, any test signals or waveforms are introduced into a signal input of DUT 21, which is different from its power supply connection and do not introduce disruptions into its power supply voltage VDD. (See column 6, lines 16-56 of Ehiro). Thus, the above-noted statement in the Examiner's Answer regarding Ehiro is incorrect.

In view of the foregoing, Appellant respectfully requests that the Board reverse the Examiner and find all pending claims allowable.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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